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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,547	04/19/2004	Lukas P.P.P. van Ginneken	SYNP 1006-0	3884

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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

MAIL DATE	DELIVERY MODE
10/20/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/828,547	VAN GINNEKEN, LUKAS P.P.P.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11,12 and 19-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11,12,19 and 20* is/are rejected.

7)☒ Claim(s) *21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application.
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/828,547 and amendment filed on 07/06/10. Claims 11, 12 and 19-21 remain pending in the application, where claims 1-10 and 13-18 are canceled.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 19 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The recitation of "preferred gains" is vague because it is not sure how a preferred gain is determined. It can be a relative term because the claim does not set forth a metes and bound of the claim limitation. One can determine gain that is preferred gain differently from other. Therefore, it is uncertainty of the claim limitation.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 11, 12 and 19-21 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-43 of U.S. Patent No. 6,453,446 and claims 1-19 of U.S. Patent No. 6,725,438. Although the conflicting claims are not identical, they are not patentably distinct from each other. 6,453,446 claiming selecting a plurality of cells from a cell library to implement a circuit path (claim 1 step (a)), determining initial delay values for the selected cells based on corresponding preferred gains (claim 1 step(a), the selected cells having an initial intended delay associated therewith for ensuring that predetermined timing constraints are met that can be suggested as preferred gains be met); prior to placement of the circuit path, determining an adjusted initial delay value by performing at least one of compressing the initial delay value or stretching the initial delay value (claim 3 recites prior to the step of routing, the area and placement of each of the selected cells and the lengths of the wires is finalized; claims 12-15 recites stretching the initial intended delay after the step of determining the placement and before the step of determining the area; compressing the initial intended delay after the step of the placement and before the step of determining area; these steps mean that stretching and compressing the initial intended delay prior to the placement of the circuit path because the placement of the cells does not include establishing a routing or placement of a circuit path; Claims 2, 5-7 describe performing assigning wire loads to the selected cells, making size area adjustment during or after placement to maintaining the initial delay value or the

adjusted initial delay and performing routing of the selected cells; claims 11-12 describe inserting a buffer. Claims 49-52 describe associating an initial gain values with each selected cell and computing initial intended delay value based on the initial intended delay value, wherein the associated gain value is reduced to compress the associated relative delay of value of the cells to assist in satisfying the predetermined timing constraints, wherein the associated gain values of the selected cells are increased to stretch the associated relative delay value of the cells to assist in reducing the area of the cells. Since the claims refereed to modeling the delay, it apparently the steps are done prior establishing a routing. It apparently that the claims of the patent anticipate or render the claims of the instant application obvious to an artisan skill in the art. The claims of 6,725,438 describe: selecting cells from a cell library to be coupled to each other, each having associated relative delay value, determining an initial intended area of each cell and lengths of wires coupled cells to meet predetermined timing constraints, prior to step of routing, finalizing the area and wire lengths, stretching the associated relative delay value of the selected cell to decrease an area of each of the selected cell delay value of each selected cell and compressing the associated relative delay value to assist in satisfying the predetermined timing constraints and the compressing is limited by a gain requirement of the selected cell; assigning loads to each cell including a net weight so that each cell selected to be placed will be met the predetermined timing constraints and performing routing. It is noted that the steps of stretching and compressing are performed prior establishing a routing or placement of a circuit path. In order to actually meet timing constraints and according to a gain requirement as

intended by design requirements, it is well known on an artisan skill in the art make some adjustment to initial delay value or some sizes of selected cells. Therefore, Examiner contends that the current claims are anticipated or obvious by the patent claims of both patents as described above.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 11, 12 and 19-20 are rejected under 35 U.S.C. 103(a) as being obvious over Li et al. (5,666,290).

8. As to claim 19, Li et al. teach an automated method for designing an integrated circuit layout with a computer, comprising:

selecting cells from a cell library to implement a circuit path (col. 9 lines 55-67; Fig. 2 shows receiving a netlist (listing of components and interconnection there between components) description of the circuit for which components are to be optimally placed; identifying driver/buffer pairs to be placed); prior to placement of the circuit path (Fig. 2 shows performing an initial placement, the initial placement does not establish or place a circuit path), determining initial delay values for the selected cells based on corresponding preferred gains of the selected cells (Fig. 2 show

computing path delays, where the path delays include determining initial delay values for the selected cells based on corresponding preferred gains of the selected cells (col. 6 lines 25-62; the slack is defined as the difference between the upper constraint on the path delay Dc, and the sum of the intrinsic delay Di of the component of each segment and the driver response delay for each segment due the sum of input capacitance Cin). determines gains of the initial delay value of the selected cells or driver to be placed);

prior to placement of the circuit path, determining an adjusted initial delay value for at least one of the selected cells (col. 8 lines 1-17; updated current placement is the input of the constraint engine which derives new path delay based on the current placement meaning performing initial delay value adjustment to meet input initial constraints) by performing at least one of:

compressing the initial delay value of at least one of the selected cells to meet delay constraints for the circuit path (col. 8 lines 1-17, performing new placement so that initial delay value will be met input initial constraints), and

stretching the initial delay value of at least one of the selected cells to reduce slack in the circuit path (col. 6 lines 26-67; col. 7 lines 1-47);

performing a placement of the selected cells for the circuit path, including assigning wire loads to the selected cells (col. 8 lines 18-53; Fig. 2 shows assign weights to nets, constant net weights specified by a user and/or derived from maximum capacitance (MAXCAP) value assigned by a user; col. 5 lines 55-60);

adjusting size or area of one or more of the selected cells during or after placement in response to the assigned wire loads, to maintain the initial delay value or the adjusted

initial delay value for the corresponding selected cells (col. 8 lines 40-57); and routing the selected cells for the circuit path (Fig. 9 show routing of the selected cells for the circuit path). Li et al. do not explicitly teach stretching or compressing the initial delay prior to the placement. However, Li et al. teach input initial constraints, identifying driver/buffer pairs, performing initial placement and computing path delays (Fig. 2). In order to meet the input constraints it would be obvious to an artisan skill in the art at the time the invention was made to perform an additional step by compressing the initial delay value of at least one of the selected cells to meet delay constraints for the circuit path or stretching the initial delay value of at least one of the selected cells to reduce slack in the circuit path prior the placement in order to meet the input constraints and making some size adjustment of the initial size of the component described in col. 8 lines 15-17) during the placement or after the placement so that the initial delay value or the adjusted initial delay value would be maintained.

9. As to claim 20, Li et al. teach, prior to placement, inserting a buffer in the circuit path when there is available slack in the circuit path (Fig. 9 show a driver or buffer 108 is inserted; col. 6 lines 13-63).

10. As to claim 11, Li et al. teach wherein the preferred gain of the cells is determined using a continuous buffering assumption (Fig. 9 show a driver/buffer pairs).

11. As to claim 12, it would be obvious to an artisan skill in the art at the invention was made to determine the initial delay value during library analysis because by doing so the initial delay value can be equally pre determined prior the routing process.

Allowable Subject Matter

12. Claim 21 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

13. The prior art of record does not teach or fairly suggest the limitations of claim 21, including prior to placement, determining net weight values for the selected cells, the net weight values representing sensitivity of total area of a circuit design to load on the corresponding cell, and determining whether to insert a buffer on the output of a given cell in the selected cells using the net weight value of the given cell.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Vuthe Siek/
Primary Examiner, Art Unit 2825